Claims

[c1] A memory array that simultaneously reads and writes different addresses of the same memory array, comprising:

a plurality of memory cells arranged in two equally sized arrays, each memory cell having a separate read and write port, wherein each port is coupled to a wordline that activates the memory cells, and a bitline that transfers data to or from said memory cells;

read bitlines and write bitlines respectively connected to a read and write port of each memory cell along a column of each of said arrays;

read wordlines and write wordlines respectively connected to the read and write ports of each memory cell along a row of each of said arrays;

a row of differential sense amplifiers wherein one sense amplifier is provided for each column of said array, and wherein each bitline from the first array being respectively attached to a first input terminal of the corresponding differential sense amplifier, and each read bitline from the second array being respectively attached to a second input terminal of the corresponding differential sense amplifier; and

a row of reference cells in each of said two arrays connected to a reference wordline and the read bitlines, wherein when the reference wordline is activated, the read bitline coupled to the activated reference cell discharges to a voltage level that is mid-way the value at which a cell stores a logic 0 and a logic 1.

[c2] The memory array of claim 1 wherein each write bitline in the first array is connected to the write bitline in the second array in the same column, enabling simultaneous read and write by activating the read wordline from the first array, the reference wordline from the second array, the write wordline from either the first or the second array and the write bitlines traversing both arrays, said arrangement resulting in transforming noise coupling from the write bitline to the read bitline into common mode noise that is rejected by said differential sense amplifiers.

[c3] The memory array of claim 1 wherein a write bitline in the first array and in the second array are respectively driven by a first and second driver having the same slew characteristics, said first and second drivers switching simultaneously.

[c4] A memory array of memory cells, each cell provided with separate read and write ports, comprising:

read and write wordlines coupling memory cells along each row of the array, read bitlines and write bitlines coupling cells along each column of the array, and differential read sense amplifiers arranged in a separate row of the array;

a read bitline pair with one read line connecting one terminal of a differential sense amplifier to a first half of the cells along a column of the array, and a second read bitline connecting the second half of the cells along the same column of the array;

a first row of reference cells connected to the first read bitline segments and a second row of reference cells connected to the second bitline segments;

a first segment of a re-entrant read bitline linking a complementary input of the differential sense amplifier to a segment of the read bitline for each column; and

a second segment of the re-entrant read bitline linking the second segment of the read bitline and extending over the first section of the array arranged symmetrically about a horizontal line at the center of the array to the second segment of the re-entrant bitline, wherein a simultaneous read and write operation is achieved by activating a read wordline in the first section of the array connected to the first bitline segment, a reference wordline in the second portion of the array, a write wordline in the first or the second section of the array and all the

write bitlines and all the differential sense amplifiers, and wherein a voltage swing on the write bitline couples an equivalent noise into all read bitline segments, thus transforming the noise into a common mode noise which is detected and rejected by the differential sense amplifiers.

[c5] The memory array of claim 4 wherein said first and second sections of the array have each the first and the second segments of said re-entrant read bitlines for each column of memory array.

[c6] The memory array of claim 4 wherein the write bitlines are driven by a row of write bitline drivers located along the periphery of the array.

[c7] The memory array of claim 4 wherein the write bitlines are driven by a row of write bitline drivers located at both the first and second edges of the array, with a first plurality of write bitlines connected to the first edge drivers and the remaining to the second edge drivers.

[c8] The memory array of claim 4 wherein the read bitlines and the re-entrant bitlines are placed on separate layers of connectivity.

[c9] The memory array of claim 4 wherein the write bitlines are on the same layer of connectivity as the read bitlines.

[c10] The memory array of claim 4 wherein the write bitlines are on the same layer of connectivity as the re-entrant bitlines

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[c11] The memory array of claim 4 wherein the write bitlines are on a layer of connectivity which is different from either the read bitlines or the re-entrant bitlines.

[c12] A memory array of dual port memory cells arranged in an array formation comprising:
memory cells in a row of said array connected to read wordlines and write wordlines, said memory cells along a column being connected by a read bitline;
an arrangement of differential sense amplifiers having each an input thereof connected to a reference voltage, the read bitline connecting all the memory cells along one column of the array to the second input of corresponding differential sense amplifier;
a write bitline provided with re-entrant connections, wherein a first segment of a write bitline is connected to half the cells along a column of the array, and a second segment of the write bitline is connected to the remaining cells along the same column of the array;
a write driver connected to and driving the first write bitline segment, and a second write driver connected to and

driving the second write bitline segment; and
input circuitry linking the write drivers , each driver simultaneously driving from and to an opposite state at a given slew rate.

[c13] The memory array of claim 12 wherein true and complement write drivers are positioned at opposite ends of the array and the arrangement of differential sense amplifiers is placed at the periphery of said array.

[c14] The memory array of claim 12, wherein the re-entrant connections link one of the write drivers to a farther write bitline segment, and the line drivers for each column of cells is connected to the write bitlines, with one-half the cells in each column being coupled to the first driver, and the remaining cells being coupled to the second driver and wherein simultaneous read and write operations are realized by activating one read wordline, one write wordline the differential sense amplifiers and all the write bitline drivers, the write bitline drivers operating for each column in a way that the output voltage of the first driver is of the same magnitude and 180° out-of-phase from the output voltage of the second driver, and wherein when the voltage on the write bitline changes, no noise is coupled from the write bitlines to the read bitlines.

[c15] The memory array of claim 14, wherein the re-entrant connections are positioned in a connecting layer that coincides with that of the read bitlines.

[c16] The memory array of claim 14, wherein the write bitline connections are positioned in a connecting layer that coincides with that of the read bitlines

[c17] The memory array of claim14, wherein the read bitlines connections are positioned in a connecting layer that differs from that of the re-entrant or write bitlines.

[c18] The memory array of claim 14, wherein a plurality of pairs of true and complement write drivers are located on one side of said array, and the remaining pairs of true and complement drivers are located on a second side of said array.